ABSTRACT

A semiconductor dynamic random-access memory device which embodies numerous features that collectively and/or individually prove beneficial and advantageous with regard to such considerations as have been described above. The disclosed memory device is a 64 Mbit dynamic random-access memory device which comprises eight substantially identical 8 Mbit partial array blocks or PABs, with each pair of PABs comprising a 16 Mbit quadrant of the device. Between the top two quadrants and between the bottom two quadrants are column blocks containg I/O read/write circuitry, column redundancy fuses, and column decode circuitry. Column select lines originate from the column blocks and extend right and left therefrom across the width of each quadrant. Each PAB in the memory array comprises eight substantially identical 1Mbit sub-array blocks or SABs. Associated with each SAB are a plurality of local row decoder circuits which function to receive partially decoded row addresses from a row predecoder circuit and to generate local row addresses which are supplied to the SAB with which they are associated. Various pre-packaging and/or post-packaging options are provided for enabling a large degree of versatility, redundancy, and economy of design. Certain programmable options of the disclosed device are programmable by means of both laser fuses and electrical fuses. In the RAS chain, circuitry is provided for simulating the RC time constant behavior of word lines and digit lines during memory accesses, such that memory access cycle time can be optimized. Test data compression circuitry is provided for optimizing the process of testing each cell in the array.

In addition, on-chip topology circuitry is provided for simplifying the testing procedure. An improved voltage generator for supplying power to the memory device is provided. The voltage generator includes an oscillator, and a plurality of charge pump circuits forming one multi-phase charge pump.